REMARKS

I. Status of Application

By the present Amendment, claim 5 has been canceled without prejudice or disclaimer. Claims 1, 3-4 and 6-7 are all the claims pending in the application. Claims 1 and 3-7 have been rejected.

II. Claim Rejections Under 35 U.S.C. § 103

Claims 1, 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over newly cited U.S. Patent Publication No. 2002/0039211 to Shen et al. (hereinafter "Shen") in view of FR 2,491,702 to Veillard (hereinafter "Veillard")[1]. Applicant respectfully traverses all of these rejections for *at least* the reasons set forth below.

As an initial matter, Applicant notes that claim 5 has been canceled without prejudice or disclaimer and, therefore, the Examiner's rejection regarding claim 5 is now moot.

Further, by way of overview, illustrative embodiments of the invention recited in claim 1 are directed to recovering a clock signal from a distorted optical signal with an improved tolerance for dispersion. As explained in the present Specification, for instance, when transmitting high bit rate optical signals in optical fibers over long distances, such transmitted optical signals are subject to dispersion and such dispersion effects reduce the optical power

[1] Applicant notes that page 2 of the 10/02/09 Office Action indicates that claims 1 and 3-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen in view of U.S. Patent Publication No. 2003/0020985 to LaGasse, but pages 3-4 of the 10/02/09 Office Action set forth grounds of rejection based on FR 2,491,702 to Veillard. Accordingly, Applicant assumes that page 2 of the 10/02/09 Office Action contains a typographical error and that the Examiner intended to indicate that claims 1 and 3-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen in view of Veillard.

within the transmitted optical signal and, consequently, it is difficult to recover a clock signal (*see e.g.,* Specification, page 2, lines 9-17).

To address these difficulties in recovering a clock signal (and other difficulties) illustrative embodiments of the invention recited in claim 1 drive a phase locked loop ("PLL") with an optical-to-electrical converted data signal filtered at $1/n$ of the bitrate and multiplied by n (n being a natural number larger than 2). As explained in the Specification, a clock signal at exactly the bit rate frequency can be generated not only by frequency doubling (n=2), but also with any higher multipliers n of the natural series, as well (Specification, page 3, lines 5-14).

Accordingly, illustrative embodiments of the invention recited in claim 1 combine a frequency filter with a transmit frequency of around B/n (wherein B is the bit rate of the electrical data signal) and a frequency multiplicator unit, which performs a frequency multiplication by a factor of n, to obtain a frequency signal with $f = B$. As a result, illustrative embodiments of the invention recited in claim 1 effectively replace a part of the frequency spectrum that is too weak for clock recovery with a spectral component having significantly higher signal power and, thus, achieve a dramatically improved dispersion tolerance.

However, neither Shen, Veillard, nor any combination thereof, teaches or suggests all the features of claim 1 and, thus, claim 1 would not have been obvious in view of the cited references for *at least* these reasons. In fact, as explained below, the teachings of Shen and Veillard are completely different than claim 1.

First, by way of overview, in contrast to claim 1 Shen teaches a device for combining a number of low-speed channels in to a high-speed channel which can maintain the original timing of the low-speed channels and also meet timing hitter requirements for each channel (*see e.g.,* Shen, paragraph 0012). While Shen does teach a clock recovery module 723, Shen provides no

teaching or suggestion whatsoever regarding driving a phased locked loop circuit of the clock recovery module 723 with a frequency-multiplied signal (*see e.g.,* Shen, FIG. 6A). Consequently, Shen cannot possibly suggest the novel combination of a frequency filter with a transmit frequency of around B/n and a frequency multiplicator unit, which performs a frequency multiplication by a factor of n, as recited in claim 1.

On the other hand, Veillard teaches a circuit for clock recovery of phase modulated digital signals so as to generate a modulation free digital signal. Contrary to claim 1, however, Veillard provides no suggestion at all regarding combining a frequency filter with a transmit frequency of around B/n and a frequency multiplicator unit, which performs a frequency multiplication by a factor of n, to recover a clock signal, as recited in claim 1. In fact, Veillard teaches away from using a filter that transmits around B/n, as claimed, since such a filter would destroy parts of the signal used for the operation of Veillard's circuit.

Therefore, since neither Shen, Veillard, nor any combination thereof, teach or suggest the claimed features, much less mention the idea of effectively replacing a part of the frequency spectrum that is too weak for clock recovery with a spectral component having significantly higher signal power to improved dispersion tolerance, Applicant respectfully submits the claim 1 would not have been obvious in view of the cited references for *at least* these reasons.

Second, turning to the specific grounds of rejection, the Examiner relies on Shen's frequency multiplier in the synchronizer 736 as allegedly corresponding to the frequency multiplicator unit recited in claim 1. Applicant respectfully disagrees and notes that claim 1 explicitly requires the features of a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal.

In contrast to claim 1, Shen's frequency multiplier in the synchronizer 736 performs frequency multiplication on the recovered symbol clock signals transmitted by the clock recovery module 723 (*see* Shen, Paragraphs 0054; 0158-0161; FIGS. 4A and 6A). Shen does not teach or suggest that the frequency multiplier in the synchronizer 736 frequency multiplies the converted electrical data signal generated by the O/E converter 220. To the contrary, Shen teaches that the converted electrical data signal generated by the O/E converter 220 is frequency division demultiplexed into a plurality of low-speed symbol channels (Shen, Paragraph 0054). The clock recovery module 723 then recovers symbol clock signals from the plurality of low-speed symbol channels, which are then rate-converted and transmitted to the frequency multiplier in the synchronizer 736. Thus, Shen fails to teach or suggest that the frequency multiplier in the synchronizer 736 frequency-multiplies the converted electrical data signal.

Claim 1 also requires that the recited frequency multiplication is an analog signal processing technique. The grounds of rejection summarily allege that FIG. 6A of Shen teaches these features (10/02/09 Office Action, page 3). Applicant respectfully disagrees and notes, in sharp contrast to the claimed invention, Shen teaches that the frequency multiplier in the synchronizer 736 performs frequency multiplication after the A/D converter 720 converts the incoming symbol channel to digital form (Shen, Paragraph 0159; FIG. 6A). Therefore, the cited references fail to teach or suggest all the features of claim 1 for *at least* these additional reasons.

Third, the grounds of rejection rely on Shen's Nyquist filter 722 as allegedly corresponding to the claimed frequency filter. Applicant respectfully disagrees and notes that claim 1 recites that the frequency filter transmits around B/n, wherein B is the bit rate of the electrical data signal. The grounds of rejection fail to identify any aspect of the cited references

that allegedly teaches or suggests these features (10/02/09 Office Action, page 3). Accordingly, the grounds of rejection are unsupported and should be withdrawn for *at least* these reasons.[2]

Further, Shen provides no teaching or suggestion whatsoever that the Nyquist filter 722 transmits around B/n, wherein B is the bit rate of the electrical data signal, as claimed. Shen teaches little more than that the Nyquist filter 722 reduces unwanted artifacts from the A/D conversion (Shen, paragraph 0159). Hence, the cited references fail to teach or suggest all the features of claim 1 for *at least* these additional reasons.

Fourth, the grounds of rejection allege that it would have been obvious to include the circuit shown in FIGS. 1 and 4 of Veillard in Shen's frequency multiplier in the synchronizer 736 so as to achieve the claimed invention. Again, Applicant respectfully disagrees and submits that, even assuming *arguendo* that one *were* to include Veillard's circuit in Shen's frequency multiplier in the synchronizer 736, one still would not arrive at the features in claim 1.

Indeed, claim 1 requires that frequency-multiplied signal (produced by the frequency multiplicator unit) is used to drive the phase locked loop circuit of the clock recovery unit. However, even if Veillard's circuit *were* included in Shen's frequency multiplier in the synchronizer 736, the resultant signal from the modified frequency multiplier in the synchronizer 736 would not drive the phase locked loop circuit of Shen's clock recovery module 723.

Further, the grounds of rejection have failed to articulate any reasoning whatsoever as to why it would have been obvious to further modify the combination of Veillard and Shen so that the signal produced by Shen's frequency multiplier in the synchronizer 736 is used to drive a

[2] "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness". KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (U.S. 2007)

phase locked loop of the clock recovery module 723. In fact, such a modification would fundamentally change the principle of operation of Shen's frequency multiplier in the synchronizer 736, which is configured to frequency multiply a symbol clock that has already been recovered so as to time the release of data from FIFO 732, rather than drive the clock recovery module 723.

Therefore, claim 1 is patentable over the cited references for *at least* these additional reasons. Moreover, the dependent claims 3-4 and 6-7 are allowable *at least* by virtue of their dependency. Thus, Applicant respectfully requests that the Examiner withdraw these rejections.

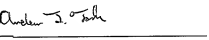
Finally, Applicant again draws the Supervisory Examiner's Attention to MPEP § 707.02 and requests that the Supervisory Patent Examiner personally check on the pendency of this application with a view to finally concluding its prosecution.

III. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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